GUJARAT TECHNOLOGICAL UNIVERSITY (GTU)

Competency-focused Outcome-based Green Curriculum-2021 (COGC-2021)
Semester -V

Course Title: Computer Organization & Architecture
(Course Code: 4350701)

Diploma programme in which this course is offered	Semester in which offered
Computer Engineering	5th semester

1. RATIONALE

This course provides details of the computer system as a whole and its functional components as part their characteristics, working principles, performance, and internal and external communication. Interactions including system bus, different types of memory and input/output organization with Processor. This course also covers hardware architectural issues and assembly language programming. On top of that, the students are also introduced to the increasingly important area of hardware evolution and working fundamentals of processor. This course provides domain specific fundamental knowledge of microprocessor as well as computer system architecture, working, characteristic and communication with peripherals which are essential for hardware related domain for all students of computer engineering and allied branches.

2. COMPETENCY

The course content should be taught and implemented with the aim to develop different types of skills so that students are able to acquire following competencies:

- **Examine computer architecture and explore assembly language programing using 8085 instructions set.**

3. COURSE OUTCOMES (COs)

The theory should be taught and practical should be carried out in such a manner that learners are able to acquire different learning outcomes in cognitive, psychomotor and affective domain to demonstrate following course outcomes.

i. Analyze computer systems at the hardware level, including CPU components & circuits, buses, and registers considering trade-offs and the evolution of processors.
ii. Examine 8085 Architecture and its working
iii. Perform Assembly language programming using 8085 Instruction Set.
iv. Characterize need of various Memory types in hierarchy
v. Visualize CPU-I/O Communication and working.

4. TEACHING AND EXAMINATION SCHEME

Teaching Scheme (In Hours)			Total Credits (L+T/2+P/2)	Examination Scheme				
				Theory Marks		Practical Marks		Total Marks
L	T	P	C	CA	ESE	CA	ESE	
3	-	2	4	30	70	25	25	150

(*): Out of 30 marks under the theory CA, 10 marks are for assessment of the micro-project to facilitate integration of COs and the remaining 20 marks is the average of 2 tests to be taken during the semester for the assessing the attainment of the cognitive domain UOs required for the attainment of the COs.

***Legends: L**-Lecture; **T** – Tutorial/Teacher Guided Theory Practice; **P** -Practical; **C** – Credit, **CA** - Continuous Assessment; **ESE** -End Semester Examination.*

5. COURSE MAP (with sample COs, PrOs, UOs, ADOs and topics)

This course map provides the student an overview of the flow and linkages of the various types of learning outcomes to be attained by the students in all domains of learning leading to the industry identified competency depicted at the center of this map.

6. SUGGESTED PRACTICAL EXERCISES

The following practical outcomes (PrOs) are the subcomponents of the COs These PrOs need to be attained to achieve the COs.

Sr. No.	Practical Outcomes (PrOs)	Unit No.	Approx. Hrs. required
1	Outline intel processor evolution.	1	2
2	Prepare 8085 Microprocessor architecture in diagram and explain it.	2	2
3	Summarize out Data Transfer Instructions and perform minimum 3 to 5 programs associated with the said concept	3	2
4	Summarize Arithmetic Instructions of 8085 with example and execute minimum 3 to 5 programs associated with said concept.	3	2
5	Summarize Logical Instructions of 8085 with example and execute minimum 3 to 5 programs associated with said concept.	3	2
6	List Input-Output Instructions of 8085 with example and execute minimum 3 to 5 programs associated with said concept.	3	2
7	Recall Machine Control Instructions of 8085 with example and execute minimum 2 to 3 programs associated with said concept.	3	2
8	List Branching and Looping instructions of 8085 with example and execute basic 2-3 programs associated with said concept.	3	4

9	Make a small poster to represent all types of memory in Memory Hierarchy.	4	4
10	Paraphrase Associative Memory in details	4	2
11	Differentiate Programmed I/O and Interrupt initiated I/O in detail.	5	2
12	List steps to carryout CPU-IOP Communication.	5	2
	Total		**28**

Note

*i. More **Practical Exercises** can be designed and offered by the respective course teacher to develop the industry relevant skills/outcomes to match the COs. The above table is only a suggestive list.*

*ii. The following are some **sample** 'Process' and 'Product' related skills (more may be added/deleted depending on the course) that occur in the above listed **Practical Exercises** of this course required which are embedded in the COs and ultimately the competency.*

iii. Course faculty can set own's rubrics for assessment.

S. No.	Sample Performance Indicators for the PrOs	Weightage in %
1	Regularity	10
2	Concept clarity	30
3	Programming logic / write up	30
4	Representation	20
5	Questions & Answers	10
Total		**100**

7. MAJOR EQUIPMENT/ INSTRUMENTS REQUIRED

a. 8085 Microprocessor kit/ Simulator of 8085

8. AFFECTIVE DOMAIN OUTCOMES

The following ***sample*** Affective Domain Outcomes (ADOs) are embedded in many of the above-mentioned COs and PrOs. More could be added to fulfill the development of this competency.

a) Update the knowledge of processor in context with hardware evolution.
b) Discover working principles of processor.
c) Develop Assembly language programming skill.
d) Examine CPU-IOP interface.

The ADOs are best developed through the laboratory/field-based exercises. Moreover, the level of achievement of the ADOs according to Krathwohl's 'Affective Domain Taxonomy' should gradually increase as planned below:

i. 'Valuing Level' in 1st year
ii. 'Organization Level' in 2nd year.
iii. 'Characterization Level' in 3rd year.

9. UNDERPINNING THEORY

Only the major Underpinning Theory is formulated as higher-level UOs of Revised Bloom's taxonomy in order development of the COs and competency is not missed out by the students and teachers. If required, more such higher-level UOs could be included by the course teacher to focus on the attainment of COs and competency.

Unit	Unit Outcomes (UOs)	Topics and Sub-topics
Unit – I **Basics of Computer Organization and Processor Evolution**	1.1. Classify Evolution of intel Processors 1.2. Prepare chart of Basic CPU Structure & Registers 1.3. Differentiate Bus Organization	1.1.1. Observe the characteristic of Intel processor from 4 bit (4004) to i7 1.2.1. Basic CPU Structure • CU, ALU and MU 1.2.2. Various Registers used in CPU & its applications • AC, DR, AR, PC, MAR, MBR, IR 1.3.1. Types of Buses used in CPU • Common / Shared Bus v/s Dedicated Bus • Serial Bus v/s Parallel Bus
Unit – II **8085 Microprocessor**	2.1. Make a chart of 8085 Microprocessor architecture and describe it. 2.2. Interpret 8085 Instruction Execution	2.1.1. 8085 Pin Diagram & Pin Functions 2.1.2. 8085 Microprocessor Architecture 2.1.3. 8085 General Purpose Registers 2.1.4. 8085 Flag Register 2.2.1. 8085 Instruction Execution ● Fetch ● Decode ● Execute operations
Unit – III **8085 Assembly Language Programming**	3.1. Describe Machine Language Instruction Format & Addressing Modes 3.2. Develop programs using 8085 Instruction Set 3.3. Classify various Interrupts of 8085	3.1.1. Instruction format opcode & Operands 3.1.2. Machine Language Instruction Format: 1-Byte, 2-Byte & 3-Byte 3.1.3. 8085 Addressing Modes 3.2.1. Data transfer Instructions 3.2.2. Arithmetical Instructions 3.2.3. Logical Instructions 3.2.4. Branching & Looping Instructions 3.2.5. Stack Instructions 3.2.6. I/O and Machine Control Instructions 3.3.1. Classification of 8085 Interrupts and its priorities 3.3.2. 8085 Vectored interrupts: TRAP, RST 7.5, RST 6.5, RST 5.5 and RST Instruction 3.3.3. 8085 Non-Vectored Interrupts: INTR

Unit – IV **Memory Organization**	4.1. Classify Memory Types and Memory Hierarchy 4.2. Differentiate types of Main memory, Auxiliary memory, Cache and Virtual Memory	4.1.1. Memory classifications 4.1.2. Memory Hierarchy 4.2.1. Various types of Main memories ● RAM ● ROM ● PROM ● EPROM ● EEPROM ● Associative Memory 4.2.2. Various types of Auxiliary memories ● Magnetic tape ● Floppy disk ● Hard Disks ● Flash Memory 4.2.3. Cache Memory 4.2.4. Virtual Memory
Unit – V **Input-Output Organization**	5.1. Explain I/O interface 5.2. Differentiate various Modes of Data Transfer with I/O 5.3. Describe Input-Output Processor (IOP) 5.4. Describe CPU-IOP communication	5.1.1. Input-Output Interface 5.1.2. Programmed I/O and Interrupt initiated I/O 5.1.3. CPU-IOP communication

***Note**: The UOs need to be formulated at the 'Application Level' and above of Revised Bloom's Taxonomy' to accelerate the attainment of the COs and the competency.*

10. SUGGESTED SPECIFICATION TABLE FOR QUESTION PAPER DESIGN

Unit No.	Unit Title	Teaching Hours	Distribution of Theory Marks			
			R Level	U Level	A Level	Total Marks
I	**Basics of Computer Organization and Processor Evolution**	04	03	3	00	6
II	**8085 Microprocessor**	10	08	08	02	18
III	**8085 Assembly Language Programming**	14	08	08	08	24
IV	**Memory Organization**	08	06	06	00	12
V	**Input/output Organization**	06	04	04	02	10
	Total	**42**	**29**	**29**	**12**	**70**

***Legends:** R=Remember, U=Understand, A=Apply and above (Revised Bloom's taxonomy)*
***Note**: This specification table provides general guidelines to assist students for their learning and to teachers to teach and question paper designers/setters to formulate test*

items/questions assess the attainment of the UOs. The actual distribution of marks at different taxonomy levels (of R, U and A) in the question paper may vary slightly from the above table.

11. SUGGESTED STUDENT ACTIVITIES

Other than the classroom and laboratory learning, following are the suggested student-related ***co-curricular*** activities which can be undertaken to accelerate the attainment of the various outcomes in this course: Students should conduct following activities in group and prepare reports of about 5 pages for each activity, also collect/record physical evidences for their (students') portfolio which will be useful for their placement interviews:

a) Plan group discussion on Various Memories available.
b) Undertake Micro-Projects in teams
c) Give a seminar on recent Processor Architectures like AMD Ryzen, Intel Core i9.
d) Plan some activities where students make charts and comparison posters on various topics and present them during the laboratory hours.
e) Ask students to get their hands on various types of memory devices like Floppy Drives, Magnetic Tapes etc. available in the old days to understand its working and the evolution from that memory to currently available disks.

12. SUGGESTED SPECIAL INSTRUCTIONAL STRATEGIES (if any)

These are sample strategies, which the teacher can use to accelerate the attainment of the various outcomes in this course:

a) Massive open online courses (***MOOCs***) may be used to teach various topics/subtopics.
b) Guide student(s) in undertaking micro-projects.
c) ***'L' in section No. 4***means different types of teaching methods that are to be employed by teachers to develop the outcomes.
d) About ***20% of the topics/sub-topics*** which are relatively simpler or descriptive in nature is to be given to the students for ***self-learning***, but to be assessed using different assessment methods.
e) With respect to ***section No.11***, teachers need to ensure to create opportunities and provisions for ***co-curricular activities***.
f) Guide students for simulator of Assembly language programming.

13. SUGGESTED MICRO-PROJECTS

Only one micro-project is planned to be undertaken by a student that needs to be assigned to him/her in the beginning of the semester. In the first four semesters, the micro-project is group-based. However, in the fifth and sixth semesters, it should be preferably be ***individually*** undertaken to build up the skill and confidence in every student to become problem solver so that s/he contributes to the projects of the industry. In special situations where groups have to be formed for micro-projects, the number of students in the group should ***not exceed three.***

The micro-project could be industry application based, internet-based, workshop-based, laboratory-based or field-based. Each micro-project should encompass two or more COs which are in fact, an integration of PrOs, UOs and ADOs. Each student will have to maintain a dated work diary consisting of individual contributions in the project work and give a seminar presentation of it before submission. The total duration of the micro-project should not be less than ***16 (sixteen) student engagement hours*** during the course. The student ought to submit a micro-project by the end of the semester to develop the industry-oriented COs.

A suggestive list of micro-projects is given here. This has to match the competency and the COs. Similar micro-projects could be added by the concerned course teacher:

- **Project Idea 1:** Identify any other microprocessor chip like 8085 prepare a model chart.
- **Project Idea 2:** Make collection of various storage devices and exhibit it in laboratory
- **Project Idea 3:** Make collection of various types of instructions sets.
- **Project Idea 4:** Make small scale Program in 8085.
- **Project Idea 5:** Collect various types of Discs and make a Chart with Explanation
- **Project Idea 6:** Prepare chart of memory hierarchy
- **Project Idea 7:** Prepare chart to show instruction pipelining
- **Project Idea 8:** Prepare chart of various processor evaluation

14. SUGGESTED LEARNING RESOURCES

Sr. No.	Title of Book	Author	Publication with place, year and ISBN
1	Microprocessor Architecture, Programming and Application with 8085	Ramesh S. Gaonkar	5th Edition, Prentice Hall
2	Computer system Architecture	Mano, M. Morris	Pearson publication, Latest Edition ISBN: 978-81-317-0070-9
3	Microprocessor and interfacing Programming and Hardware	Douglas V. Hall	McGraw-Hill International Edition.
4	Computer Architecture and Organization	Ghoshal, Subrata	Pearson publication, Latest Edition
5	Computer Architecture	Parhami, Behrooz	Oxford publication, Latest Edition ISBN: 978-0-19-808407-5

15. SOFTWARE/LEARNING WEBSITES

a. http://www.ddegjust.ac.in/studymaterial/msc-cs/ms-07.pdf
b. http://www.iitg.ernet.in/asahu/cs222/Lects/
c. http://www.srmuniv.ac.in/downloads/computer_architecture.pdf
d. https://www.oshonsoft.com/8085.php
e. Sim8085 - A 8085 microprocessor simulator
f. https://www.sim8085.com/
g. https://youtu.be/8c6K0a8xC8w (for intel processor evolution -sample web resource)

16. PO-COMPETENCY-CO MAPPING

Semester V	Computer Organization and Architecture (4350701)						
	POs and PSOs						
Competency & Course Outcomes	**PO 1 Basic & Discipline specific knowledge**	**PO 2 Problem Analysis**	**PO 3 Design/ development of solutions**	**PO 4 Engineering Tools, Experimentation &Testing**	**PO 5 Engineering practices for society, sustainability & environment**	**PO 6 Project Management**	**PO 7 Life-long learning**
Competency **Examine computer architecture and explore assembly language programing using 8085 instructions set**							
Explain Generic Computer and ALU Architecture and processor Evolution.	2	2	2	1			2
Examine 8085 Architecture and its working	3	3	2			1	2
Perform Assembly language programming using 8085 Instruction Set.	2	2	2	2		2	2
Explain various Memory types in hierarchy and their needs	3	2	1			1	1
Test CPU-I/O Communication and working.	2	1	1				1

Legend: '**3'** for high, '**2**' for medium, **'1'** for low or **'-'** for the relevant correlation of each competency, CO, with PO/ PSO

17. COURSE CURRICULUM DEVELOPMENT COMMITTEE

GTU Resource Persons

Sr. No.	Name and Designation	Institute	Email
1	Mr. S. B. Prasad	Government Polytechnic Gandhinagar	sbprasad011@gmail.com
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